Abstracts

A CMOS 6-bit, 1 GHz ADC for IF sampling applications

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The design plan and measurement results of a very high speed 6-bit CMOS Flash Analog-to-digital converter (ADC) are presented. The very high acquisition speed is obtained by improved comparator design and optimized pre-amplifier design. At these high frequencies power-efficient error correction logic is necessary. Measurements show the high conversion speed of the ADC. Maximum acquisition speed is above 1 GHz.

❑ Return to main document.